CHES™ Foundations

Series Part 2: Sapphire That Scales

This white paper examines the benefits of CHES sapphire growth technology and its use for large diameter substrates in high-brightness LED manufacturing.

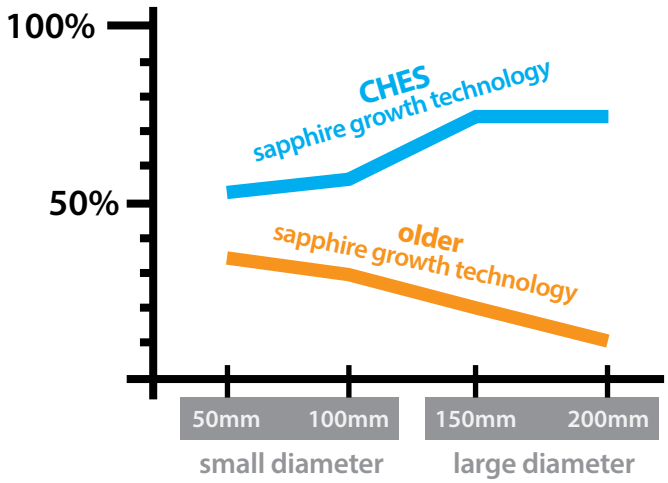
Executive Summary

It is universally accepted that larger diameter substrates are required for the growth of the high-brightness LEDs (HB-LED) market. However, common older sapphire growth technologies become less cost-effective as substrate diameters increase.

This is why ARC Energy created a paradigm shift with the new CHES™ (Controlled Heat Extraction System) technology, where manufacturing efficiency of product from sapphire crystals increases as the substrate size increases. With CHES, sapphire is grown directly on the c-axis of the crystal for consistently high material utilization. This is achieved while retaining the quality characteristics required for LED manufacturing.

Therefore, CHES furnaces and technology are positioned as the solution of choice as the HB-LED industry moves to large diameter sapphire substrates.

Sapphire Material Utilization



The fundamental advantage of CHES: consistently high sapphire material utilization, which brings lower costs for producing large diameter substrates.

CHES furnaces and technology are positioned as the solution of choice as the HB-LED industry moves to large diameter sapphire substrates.

Introduction

The long-term benefits of solid state lighting (SSL) are clear: lower energy costs, longer life, better light, and more flexibility. Yet mass adoption has been slowed because prices are still too high. Solutions must be developed to reduce costs.

A key component for significant cost reduction is to manufacture LED chips on large substrates of 150mm (6 inches) diameter and larger. The silicon industry made this transition over twenty years ago and gained extra benefits in automation and tracking. Section 1: Benefits of Large Diameter Substrates covers these topics.

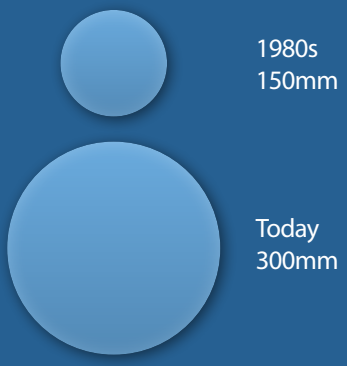
Creating larger wafers presents significant barriers for older sapphire growth technologies. The combination of low a-axis growth material utilization and unavoidable defects severely lowers overall utilization. Wafers created using older sapphire growth technology also have stress and strain variations that can result in more bow and warp during LED manufacturing. These factors are explained in Section 2: Older Sapphire Growth Technology.

These barriers to growth have created a need for new approaches to sapphire growth, such as CHES technology. CHES furnaces are designed for consistently high material utilization, which becomes even more favorable as core diameter increases. The advantages of CHES technology for large diameter sapphire growth in today's marketplace are explained in Section 3: Sapphire That Scales: CHES Sapphire Growth Technology.

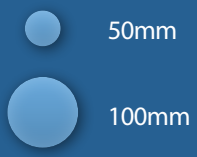
Wafer Size History

While HB-LED substrates are commonly made on 50mm-100mm wafers, this size was obsolete over twenty years ago in the silicon industry.

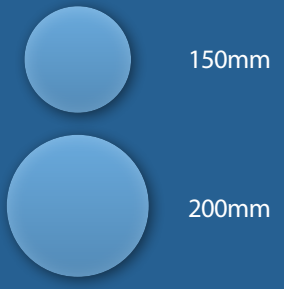
Silicon wafer sizes, then and now:



Small diameter HB-LED wafer sizes:



ARC Energy's CHES furnaces are optimized for large diameter wafers:



Section 1: Benefits of Large Diameter Substrates

A key factor in reducing HB-LED chip prices is increasing wafer size. Moving to large diameter wafers will create many more LED chips per MOCVD run. We will examine the reasons for this using examples from typical MOCVD configurations.

More LED Chips per Wafer

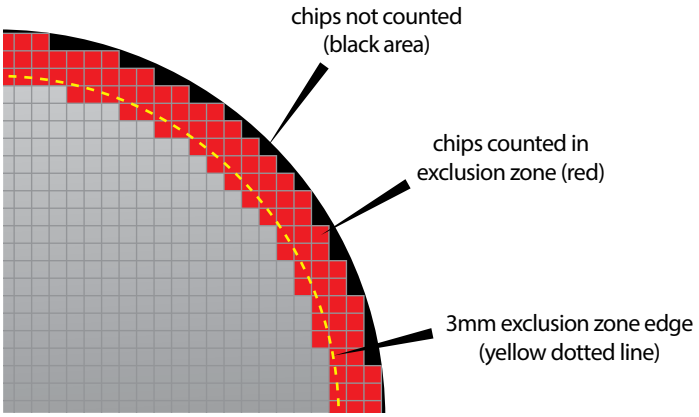
Each 50mm increase in wafer diameter results in a significant increase in wafer surface area. A 150mm wafer has nearly nine times the gross surface area of a 50mm wafer (actual dimension is 50.8mm).

However the advantage is even higher when you consider that wafers have a 3mm "exclusion zone" near the edge of the wafer. As wafer surface area grows, the exclusion zone grows, but at a slower rate. As a result, a 150mm wafer actually has not just nine times more area but 10.3 times more than 50mm. The relationship between gross surface area and the net after accounting for the exclusion zone is shown the chart on the next page.

A further advantage at the wafer level comes when you simulate the LED chips on the wafer. We have simulated a layout of 45x45mil chips as this size is typical for HB-LEDs. As you can see in the diagram, we considered a chip as excluded (red) if it lands within or crosses the exclusion zone (standard 3mm shows as a yellow dotted line). Chips falling partially outside the wafer (black area) were not counted in the exclusion totals.

Due to larger diameter wafers having less exclusion zone curvature relative to the grid of LED chips, fewer are discarded per surface area. As the industry uses increasingly larger chip sizes to improve lumens per watt performance, there will be more chips lost per surface area when using small diameter wafers.

How We Calculate LED Chip Counts

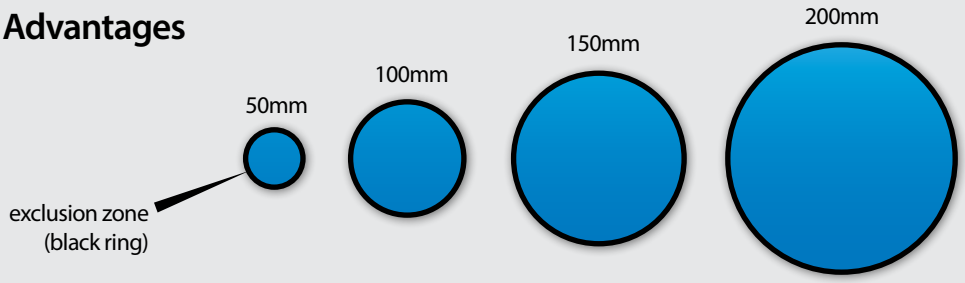


45x45mil LED chips, showing red for excluded chips and gray for included chips. Black areas are not factored in either excluded or included counts.

The combination of gross surface area with more efficient exclusion zones and relative curvature are summarized in the chart below. As you can see, a 150mm wafer carries a net advantage of 10.9 times more LED chips than 50mm (simulated using 45x45 mil chips). For 200mm, it grows to 19.8 times more.

These advantages are the fundamental building blocks for creating more LED chips per MOCVD run.

Large Diameter Wafer Advantages



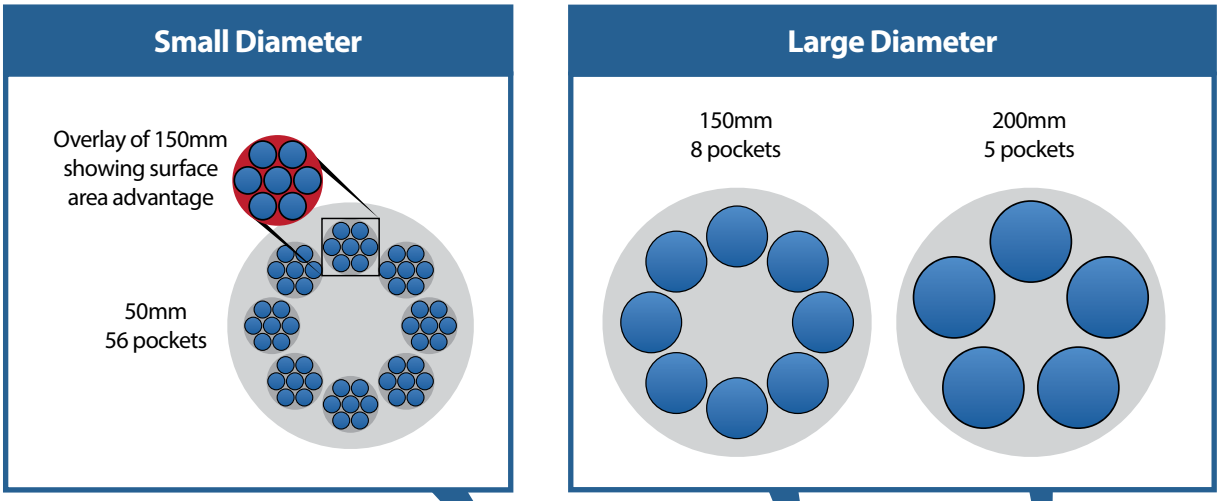
Gross surface area advantage over 50mm	-	4X	9X	16X
Surface area % lost to 3mm exclusion zone	22%	12%	8%	6%
Net surface area advantage over 50mm	-	4.4X	10.3X	18.8X
Net LED chip count advantage over 50mm	-	4.6X	**10.9X**	**19.8X**

Next we will see how these large diameter wafer advantages work in the MOCVD reactor environment. This is important because the reactor can handle many more small diameter wafers than large, so showing the final advantages of large diameter in an MOCVD run must include these factors.

More LED Chips per MOCVD Run

As we have seen, larger diameter wafers carry significantly more LED chips. Yet for a single MOCVD run—one of the most expensive parts of the LED manufacturing process—a larger number of small diameter wafers can be loaded. Therefore we must look at how fewer large diameter wafers can still result in more total LED chips per reactor run. We will now look at the actual reactor configurations for 50mm, 150mm, and 200mm wafers.

The diagram below shows three common MOCVD reactor configurations, including small and large diameter wafers. As you can see in the inset, a single 150mm wafer has much surface area (in red) than a group of seven 50mm wafers. The table shows the relative gains for large diameter configurations.



	56x50mm (2")	8x150mm (6")	5x200mm (8")
Net surface area	88,274 mm^2	130,288 mm^2	147,796 mm^2
Surface area gain vs. 50mm	-	48%	67%
Count of 45x45mil LED chips	62,944	97,600	111,280
LED chip count gain vs. 50mm	-	55%	77%

The gains in surface area and simulated chip count are significant. For 150mm, 55% more LED chips can be produced with the same cost for MOCVD supplies. As you can see 200mm is even higher. A recent study published as part of a US Department of Energy report[1] found a similar benefit of 52% for 150mm over 50mm. **This is the fundamental advantage of large diameter wafers.**

Section 2: Older Sapphire Growth Technology

Commonly used sapphire growth technology was designed decades ago and is extremely inefficient, losing 2/3rds of the sapphire grown even in the best conditions[2].

Old technology produces sapphire boules with higher concentrations of large bubbles and other defects, which create exclusion areas within the bulk of the wafers. These defects can be avoided by selecting areas with small diameter cores, but at large diameter they cannot be avoided, hence they can severely affect yield. In addition, coring perpendicular to growth results in wafers with variations in stress and strain layers across the surface of the wafer, affecting bow and warp during epitaxy.

Key Technology Differences

Older Sapphire Growth Technology	CHES Sapphire Growth Technology
• A-axis growth	• C-axis growth
• Defects throughout boule	• Very low defects for all core sizes
• Material utilization: 35% or lower, 10-20% for large diameter	• Material utilization stays high with large diameter: 75+%

Fundamental Challenges of Older Sapphire Growth Technology

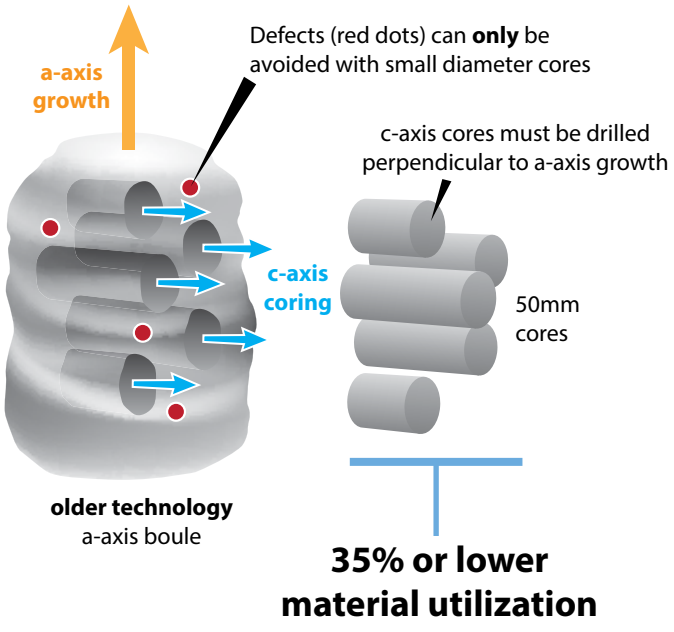
There are two fundamental challenges with older sapphire growth technologies for c-plane wafers: a-axis growth and high number of defects.

Challenge 1: A-axis Growth

As seen in the diagram, c-axis cores (required for HB-LEDs) must be extracted perpendicular to a-axis growth. Some cores are very short because they are near the edge of the boule shape, contributing to the low material utilization.

Challenge 2: High Defect Rate

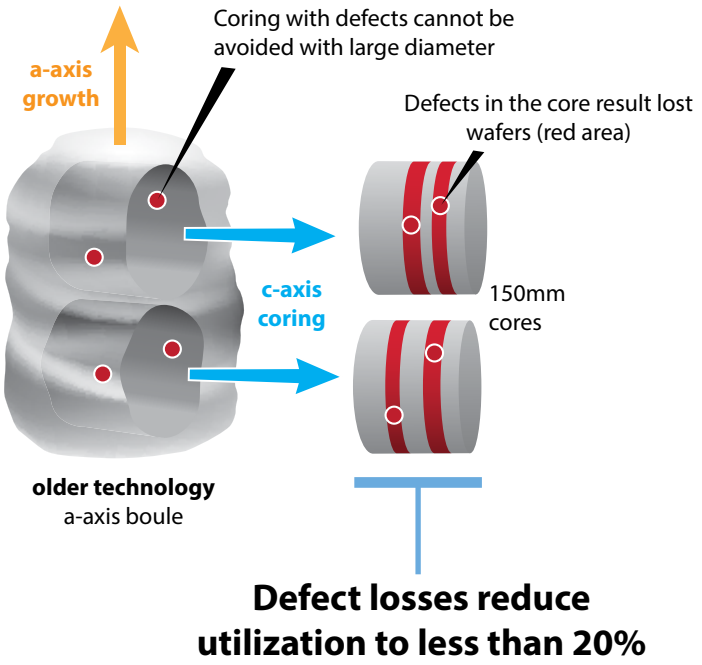
While older sapphire technology proponents claim they are defect-free, they are actually referring to using small diameter cores to avoid defect areas. This is no longer possible when using large diameter cores. In the diagram above, each red dot represents a defect area. For small diameter cores, these areas can be avoided because so much of the boule gets discarded. The best expected material utilization for this boule is 35% or lower.

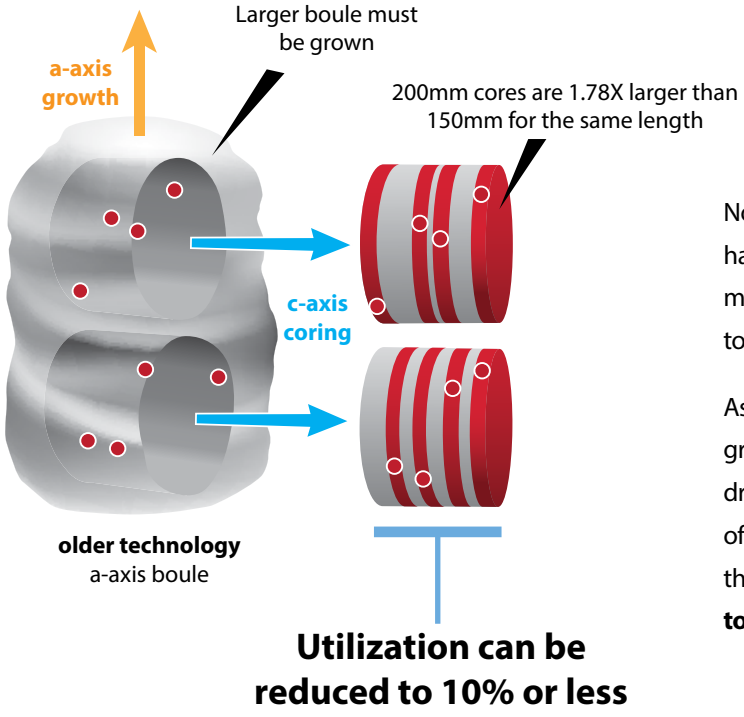


Older Technology Utilization Drops for Large Diameter

We have seen how a-axis growth limits utilization to 35% or lower when defects are avoided. Now we will see what happens with older technology when using large diameter cores.

The next boule is the same size as from the previous example, except the cores are large diameter: 150mm. You can see that there is no way to avoid the defects, so now they will be in the core and create exclusion zones (red bands). Wafers from these zones must be discarded, reducing total yield to less than 20%.





Now we are looking at 200mm cores, which have 78% more material by volume. This means the boule itself must be much larger too—with a corresponding jump in defects.

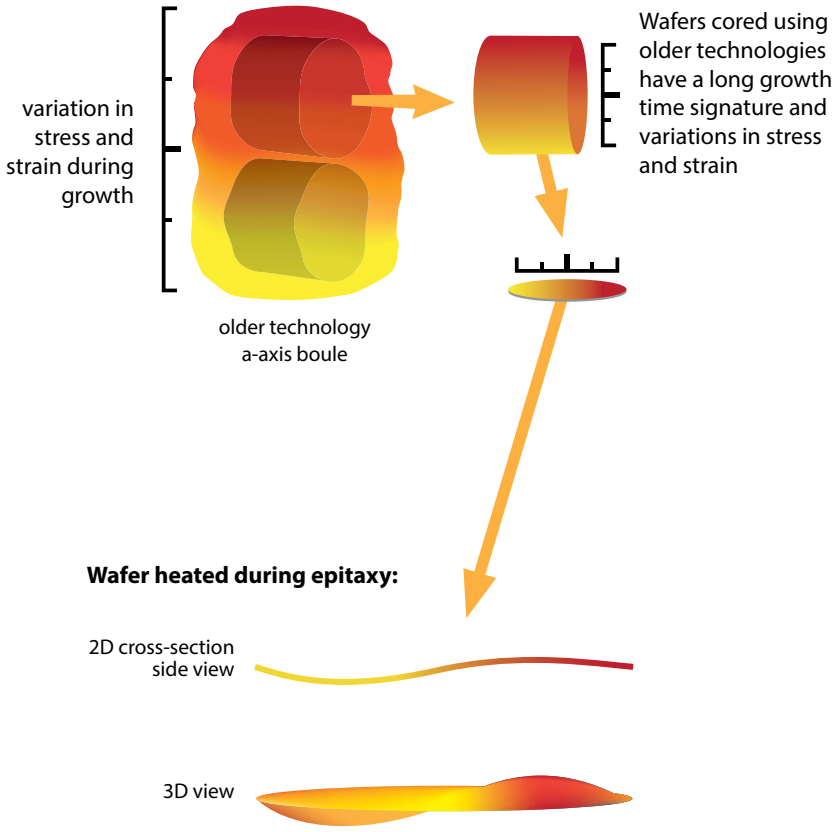
As you can see the number of defects again greatly affects the yield, which has now dropped to near 10%. If you look at the cost of growing this larger boule coupled with the lower yield, you find that **costs double to go from 150mm to 200mm.**

Wafer Bow and Warp Issues

As a sapphire boule is grown, there is an inherent variation in stress and strain in the direction of growth. Because older sapphire technology cores perpendicular to the growth plane, each wafer has a large growth time signature and contains large variations in stress and strain as shown in the diagram.

The stress and strain variations become an issue when the wafers are heated in the MOCVD reactor. There is some level of bow with any sapphire wafer. However, large variations in stress and strain can make the bow more pronounced or warp. This effect is shown in the diagram as a cross-section side view and in 3D.

Due to these issues, techniques have been attempted for 150mm wafers, including using thicker wafers to reduce bow and inserting stress-relieving layers in the epitaxy process. Both of these add to the cost of the LED chip, making them less suitable long-term solutions.



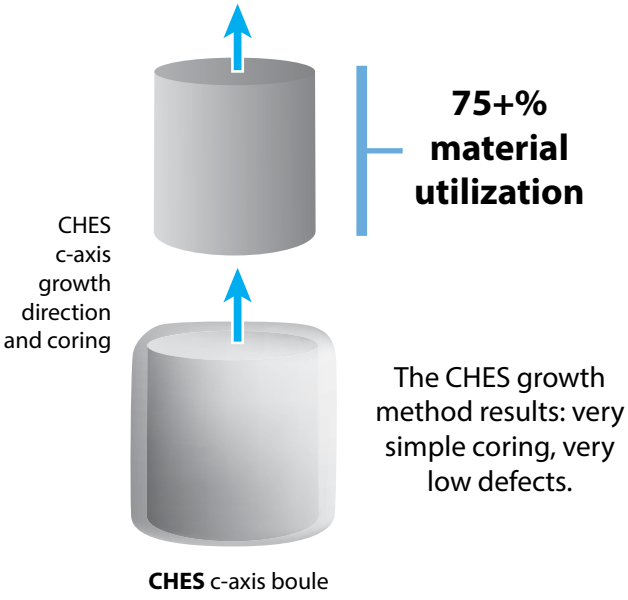
Older sapphire growth methods have severe limitations when scaling to large diameter as we have seen. The key factors are a-axis growth, defects throughout the boule, and wafer bow and warp issues during epitaxy. **The older technology is therefore not preferred as it does not scale well to provide large diameter HB-LED substrates.**

Section 3: Sapphire That Scales: CHES Sapphire Growth Technology

CHES technology was developed anticipating the coming need for high volumes of large diameter wafers. Through innovative technology, a CHES sapphire boule utilizes more than 75% of material for large diameter HB-LED applications. Each CHES-grown wafer has the same time and temperature signature—vitally important for large diameter wafers in the MOCVD process, which is sensitive to warp and bow. In addition, a single CHES furnace supports 50mm-200mm (2-8 inch) diameters with only a crucible change. These advantages mean CHES is the sapphire technology that is built to scale with the industry's move to large diameter wafers.

C-axis and High Yield Growth

As we saw in section 2, commonly used crystal growth occurs on the a-axis, with coring perpendicular to the growth axis for c-plane wafers. CHES furnaces grow directly along the c-axis and grow a nearly cylindrical boule. This provides for minimal waste and simple core extraction. In fact, typical material utilization on 150mm and 200mm diameters is 75% or higher. The diagram shows how c-axis growth from CHES provides outstanding yield.



Sapphire That Scales

With a consistent material utilization of 75% or higher across all large diameter sizes, CHES is the only sapphire technology that scales efficiently to larger sizes. If you calculate the cost increase for growing 200mm vs. 150mm with CHES, the increase is only 25%. As we saw in the previous section, a-axis growth technology needs twice the cost for this same increase.

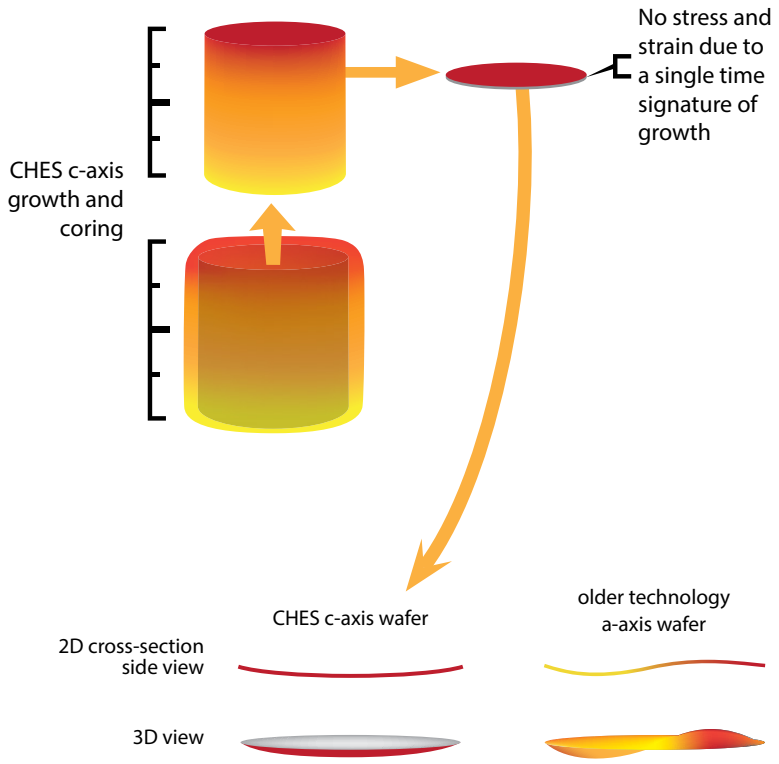
CHES furnaces can grow up to 250mm (10 inch) diameter cores and feature the ability to switch between core sizes with only a crucible change.

Reduced Stress and Strain

As we saw in section 2, a-axis growth results in c-axis wafers with large time signatures and large variations in stress and strain. CHES solves this problem as each wafer is grown along the c-axis, which results in less stress and strain within each wafer.

Because stress and strain can create additional bowing and warp issues during epitaxy, CHES sapphire is at an advantage. With large diameter wafers, the advantage is even more pronounced.

A secondary benefit to having less bow and warp is that thinner wafers can be used. Thicker large diameter wafers have been required in the past to compensate for bow and warp, in addition to expensive techniques to add stress-reducing layers in the epitaxy process. With thinner wafers, costs can be reduced significantly.



With CHES, wafers exhibit less bow and warp during epitaxy.

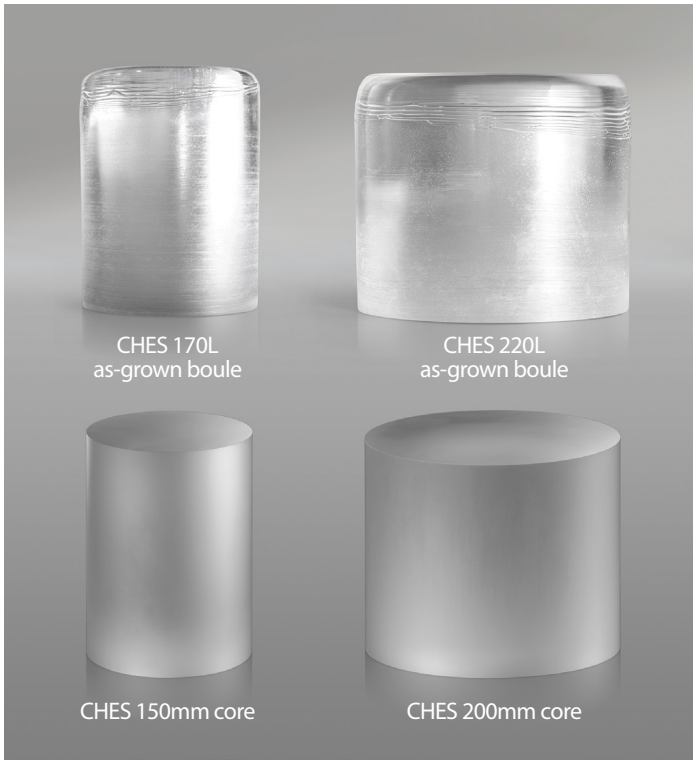
As we have seen, CHES sapphire growth technology is fundamentally different from older a-axis growth methods. The advantages are consistently high material utilization and better bow and warp performance for epitaxy. **These advantages show CHES technology and furnaces are the best solution for crystal growers seeking to compete in the HB-LED large diameter sapphire substrate market.**

Conclusions

There are clear benefits in moving to larger diameter substrates. LED chip counts jump 55% when comparing 150mm to 50mm for the same MOCVD run. For 200mm, the advantage is 77%. In addition, larger LED chips can be produced efficiently.

The barrier to wide scale adoption of large diameter is in older sapphire growth technology. Designed decades ago, this technology grows material using a bulk approach that degrades as diameter increases.

CHES technology has been created to solve the sapphire growth problems without compromising on wafer quality. The CHES furnace achieves 75% or more material utilization across all large diameter sizes. CHES technology and furnaces are therefore the clear solution to provide cost-effective large diameter sapphire substrates for the HB-LED industry.



CHES furnaces produce low defect net shape boules in large diameters.

To learn more about CHES technology and furnaces, visit ARC Energy on the web at http://www.arc-energy.com.

References

1. US Department of Energy, "Life-Cycle Assessment of Energy and Environmental Impacts of LED Lighting Products, Part 2: LED Manufacturing and Performance," p. 15.
2. Yole Développement, "Sapphire Market 2011," p. 126 "Overall Yield."

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About ARC Energy

Headquartered in Nashua, N.H., the Advanced RenewableEnergy Company, LLC (ARC Energy), was founded in 2007 to commercialize cutting edge technologies for LED and other clean energy markets. ARC Energy provides highly automated and efficient sapphire crystal growth and processing systems to enable rapid scale production and cost reduction of LEDs. For additional information about ARC Energy, please visit www.arc-energy.com.